Performance Improvement of Millimeter wave Circuits for 5G Applications

Poster Id: 91

Subbareddy Chavva, Research scholar and Dr. Immanuel Raja, Assistant professor

Department of Avionics, Indian Institute of Space Science and Technology, Thiruvananthapuram, India.

Motivation & Objective

The performance of millimeter-wave circuits in 5G applications is strongly correlated to the performance of on-chip inductors. Enhancing the quality factor (Q) of the inductors, along with improving the linearity and efficiency of the circuits, improves the overall performance.

1. Proposing various techniques for quality factor enhancement of on-chip spiral inductors and techniques to reduce the area occupied by the inductors used at millimeter-wave frequencies.
2. Design of a 28 GHz transmitter with high linearity and output power in silicon CMOS for 5G applications.

Quality factor Enhancement Techniques

1. Optimization of Guard ring Spacing

Introduction

- The effect of changing the guard ring spacing (S_g) on the performance metrics of single-turn octagonal inductor is studied.
- Four different sized inductors (30pH, 50pH, 80pH and 200pH) used at mm-wave frequencies are considered for the analysis.

Theoretical Analysis

- Model - Two inductors magnetically coupled to each other.
- Signal loss due to guard ring current from inductor- Quality factor degradation
- The guard ring current (I_g) reaches its first maximum and first minimum at,

$$\frac{l_g}{\lambda_{Igmax}} \approx 0.42 \quad \text{and} \quad \frac{l_g}{\lambda_{Igmin}} \approx 1.12$$

Where, l_g is guard ring length.

- Q degrades sharply at,

$$f_{Igmax} = \frac{0.42c}{l_g\sqrt{\epsilon_{r,eff}}}$$

Where,

$l_g \approx 4(d_{out} + 2S_g) - 2\ \mu m.$

- Q is expressed as,

$$Q = Q_0(1 - KI_g)$$

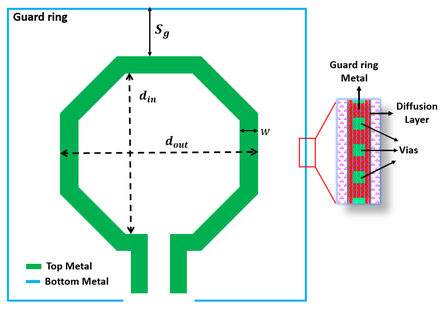


Fig.1. A typical octagonal single turn spiral inductor surrounded by guard ring.

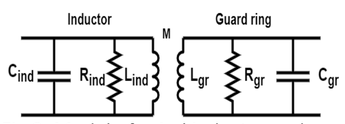


Fig.2. Model of spiral inductor and guard ring surrounding it at high frequencies.

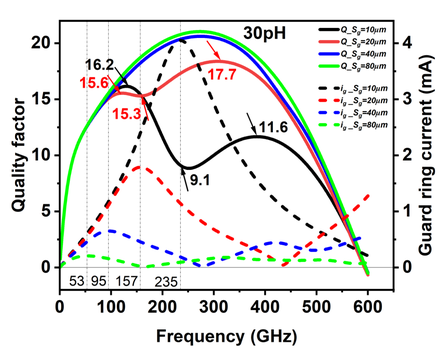


Fig.3. Plot of guard ring current and quality factor of the 30pH inductor with respect to frequency for various values of Sg.

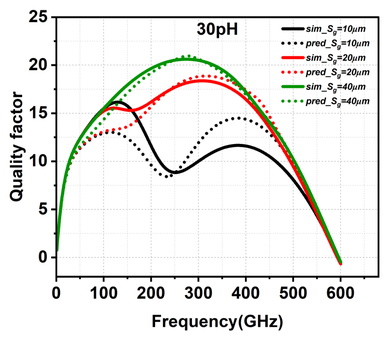


Fig.4. Plot of the simulated Q and predicted Q for 30pH inductor for various values of Sg.

Conclusion

- Significant improvement in Q with change in S_g at higher frequencies.
- Improvement in Q is relatively less for larger inductors.
- L and f_{SR} are unaffected

*Chavva Subbareddy, Immanuel Raja. "Enhancing on-chip performance of single-turn octagonal inductor at millimeter wave and Sub-THz frequencies through grounded guard ring optimization." *AEU-International Journal of Electronics and Communications* (2023): 154817.
(Elsevier Q1 journal with IF 3.2 and cite score 7.2)

2. N-well Patterning in the p-substrate

Introduction

- Quality factor of on-chip inductors is improved through n-well patterning on a p-type substrate in a typical CMOS process.
- Two styles of patterning structures are proposed.

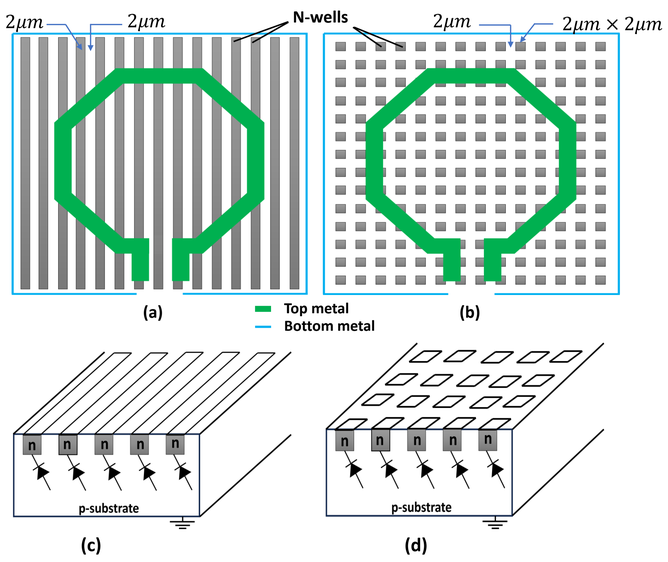


Fig. 5: Single turn octagonal spiral inductor with N-well patterned structures in the substrate. (a) Structure-1 with vertically oriented strips of n-well (b) Structure-2 with small islands of n-well (c) Cross-sectional view of structure-1 (d) Cross-sectional view of structure-2.

Analysis

- The floating n-wells form unbiased p-n junction diodes with the p-substrate.
- The unbiased diodes form electrical obstruction (high impedance) on the substrate.
- Eddy currents and capacitive coupled currents reduced.
- Eddy current resistance equation [1],

$$R_{eddy} \approx \frac{\sigma_{sub}}{4e}(\mu n f)^2 d_{avg}^3\, \rho^{0.7}\, z_{n,ins}^{-0.55}\, z_{n,sub}^{0.1}$$

Measurements

- Inductors are fabricated on a commercial 180nm CMOS process.
- Wafer probing
- SOL (Short- Open-Load) de-embedding method.
- S_{11} measurement up to 40 GHz

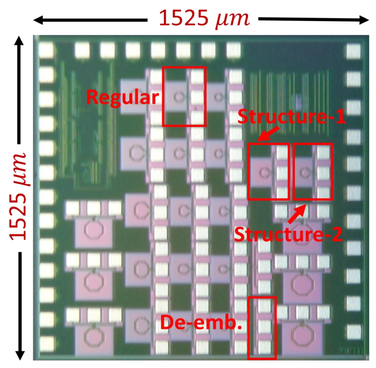


Fig.7. Micrograph of the chip, indicating and labelling the three test inductors referred, along with their de-embedding structure.

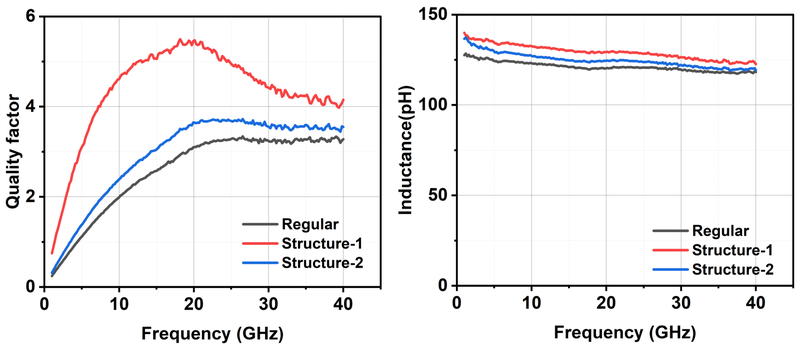


Fig.8. Plots of measured quality factor and inductance against frequency for the 120 pH regular inductor and the two inductors with n-well patterned structure-1 and structure-2.

Table 1: The comparison of the measured parameters

Patterning Technique/ Parameter	N-well patterned Structure-1 @20 GHz (This work)	N-well patterned Structure-2 @20 GHz (This work)	Poly silicon PGS @ 2 GHz [2]	n+ diffusion PGS @ 1 GHz [3]	Partial poly silicon PGS @ 4.2 GHz [4]
L (Regular/ with PGS)	**120pH/ 130pH**	**120pH/ 125pH**	7.5 nH/ 7.4 nH	4.8 nH/ 4.81 nH	-
Q (Regular/ with PGS)	**3.1/ 5.5**	**3.1/ 3.6**	5.08/ 6.76	-	6.12/ 9.58
% change in L	**8 %**	**4 %**	-1 %	0 %	-
% change in Q	**77 %**	**16 %**	33 %	21 %	56 %

Conclusion

- Quality factor improved without degrading the self-resonant frequency.
- Improvement in Q with structure-1 is better than with structure-2.
- Proposed technique is better than other PGS techniques.

*Under review

Experimental Analysis of Irregular shaped On-chip Inductors

Introduction

- Irregular shaped spiral structures are proposed for on-chip inductors used in mm-wave applications.
- The irregular shaped inductors (60pH, 80pH and 120pH) are taped out in a 180nm CMOS process and measured for their Q and inductance values.

1. Horizontal Outer diameter Expansion

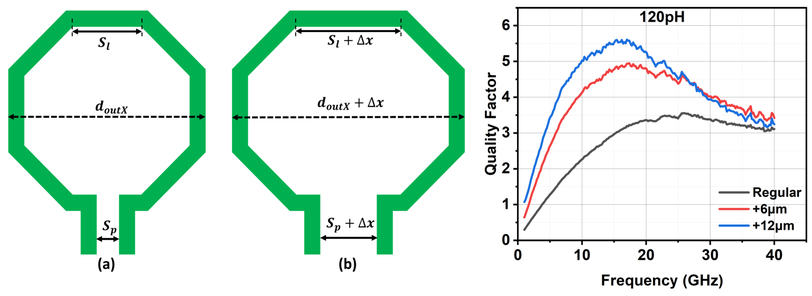


Fig.9 (a) Regular octagonal Inductor (b) Horizontal outer diameter expansion of the inductor

2. Vertical Outer diameter Shrinking

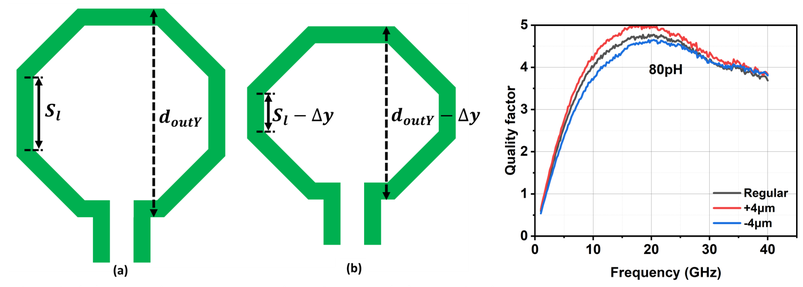


Fig.10 (a) Regular octagonal Inductor (b) Vertical outer diameter shrinking of the inductor

3. Port Spacing

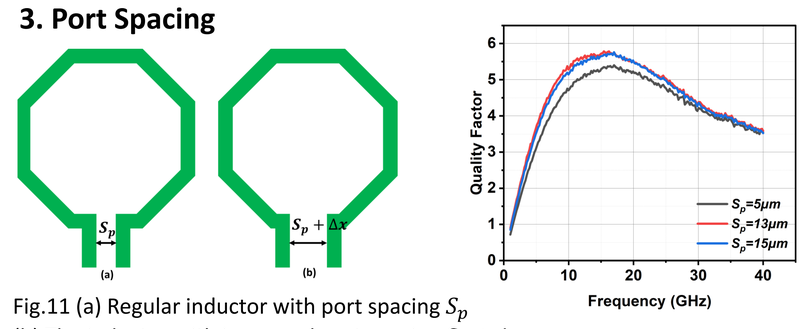


Fig.11 (a) Regular inductor with port spacing S_p (b) The inductor with increased port spacing $S_p + \Delta x$

Table 2: Comparison with equivalent regular octagonal inductor (80pH) at 20GHz

Inductor	Reg+ H4	Reg. Equi.	Reg- V4	Reg. Equi.
Sidelength	18μm	19μm	18μm	17.1μm
L (pH)	81.9	81.1	71.6	71.6
Q	16.6	17.2	15.6	16

Conclusion

- Q is not affected much with irregular shapes.
- These shapes can be used instead of the regulars to fit in the layout requirements.

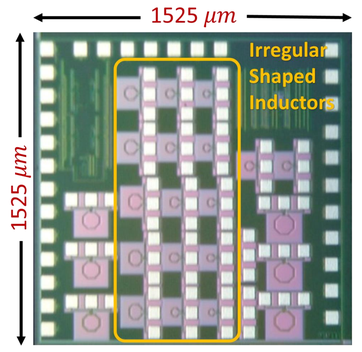


Fig.12 Micrograph of the chip, taped out in a 180nm CMOS, indicating and labelling the test inductors.

*Manuscript under preparation

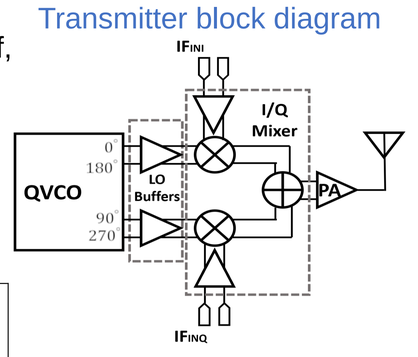
28 GHz Transmitter design in 65nm CMOS for 5G Applications*

Introduction

The transmitter constitutes of,

1. Quadrature VCO,
2. LO Buffers & I/Q Mixer ,
3. Power Amplifier

Transmitter block diagram



Simulation Results

I/Q mixer:

CG (dB)	P1dB@Vin (mV)	NF (dB)	S11 (dB) @100MHz
1.1	191	10.9	-27

Power Amplifier:

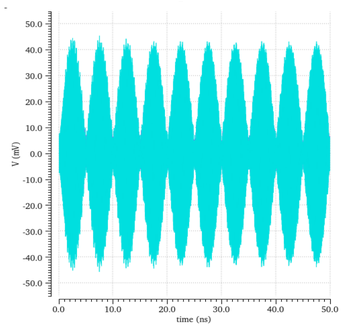


Fig. Transient response of power amplifier output.

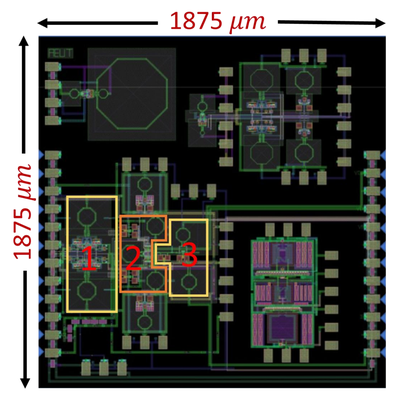


Fig. Micrograph of the chip, taped out in 65nm silicon CMOS.

*Ongoing work

Acknowledgements

Dr. Immanuel Raja acknowledges the support of the Science and Engineering Research Board (SERB), Department of Science and Technology (DST), Government of India for supporting this work in part under the SERB Start-up Research Grant (SRG/2020/002003) and the support of IIST under the IIST-Fast-Track project scheme (2020AVFSTK015).

References

1. Lee TH. The design of CMOS radio-frequency integrated circuits. Cambridge university press; 2003 Dec 22.
2. Yue CP, Wong SS. On-chip spiral inductors with patterned ground shields for Si-based RF ICs. IEEE Journal of solid-state circuits. 1998 May;33(5):743-52.
3. Chen YE, Bien D, Heo D, Laskar J. Q-enhancement of spiral inductor with N/sup+/-diffusion patterned ground shields. In2001 IEEE MTT-S International Microwave Sympsoium Digest (Cat. No. 01CH37157) 2001 May 20 (Vol. 2, pp. 1289-1292). IEEE.
4. Lin YS, Chen CZ, Liang HB, Chen CC. High-performance on-chip transformers with partial polysilicon patterned ground shields (PGS). IEEE transactions on electron devices. 2006 Dec 26;54(1):157-60.